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1 Overview

The ISL34340 evaluation kit enables the user to exercise the serdes in a lab environment and to see the high speed and parallel signals conveniently on an oscilloscope. The contents of the kit are shown in Figure 1.

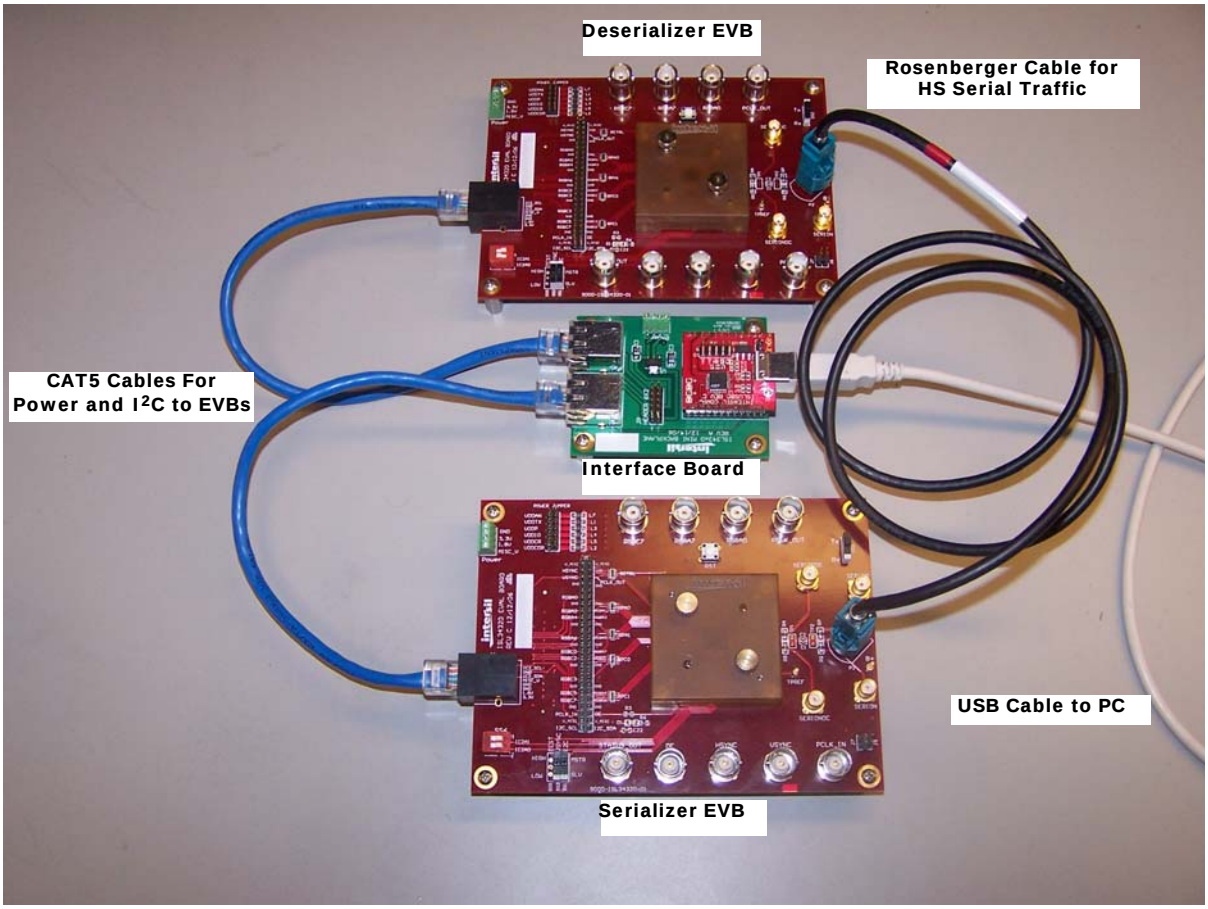


FIGURE 1. KIT CONTENTS

Schematics and software can be downloaded from:

http://www.intersil.com/data/EV/ISL34340_Eval_Kit_Software.zip

1.1 Nomenclature

For user convenience, many connectors and switches on the evaluation board are labeled with the device pin name. However, occasions arise when we need to distinguish between the connector and the device pin. The following nomenclature is adopted when specificity is needed:

TABLE 1. NOMENCLATURE

Shorthand	Refers to:	Why so specific?
ser.PCLK_IN	PCLK_IN device pin. Serdes is in video serializer mode.	We are referring to the device pin specifically and not the BNC connector. There are several paths on the EVB to the device pin.
serEVB.PCLK_IN	BNC connector labled PCLK_IN. Serdes is in video serializer mode.	This BNC is factory configured to be a sense output.
des.PCLK_IN	PCLK_IN device pin. Serdes is in video deserializer mode.	We are referring to the device pin specifically and not the BNC connector. There are several paths on the EVB to the device pin.
desEVB.PCLK_IN	BNC connector labeled PCLK_IN. Serdes is in video deserializer mode.	This BNC is factory configured to be a high impedance input.

The evaluation boards also have provision for user customization. Unless otherwise indicated, all discussion of functions and settings assume the evaluation boards are in the factory shipped state.

1.2 User Equipment Required

The serializer needs video of the proper format to function (see ISL34340/240 Technical Brief). Such signals may be provided by either attaching a raw RGB driver to J20 using a ribbon cable or by driving VSYNC, HSYNC, and PCLK pins on J20 (not BNCs) using additional function generators. The BNC connectors on the serializer board are sense “outputs” only, to hook up to scopes.

An LCD panel may be connected to J20 to view the deserializer video output.

Other equipment required is as follows:

- 3.3V Power Supply, 1A.
- 50MHz function generator
- Windows PC with USB
- 500MHz oscilloscope

1.3 Evaluation Board

Each kit contains 2 evaluation boards (EVB); one for the serializer and another for the deserializer.

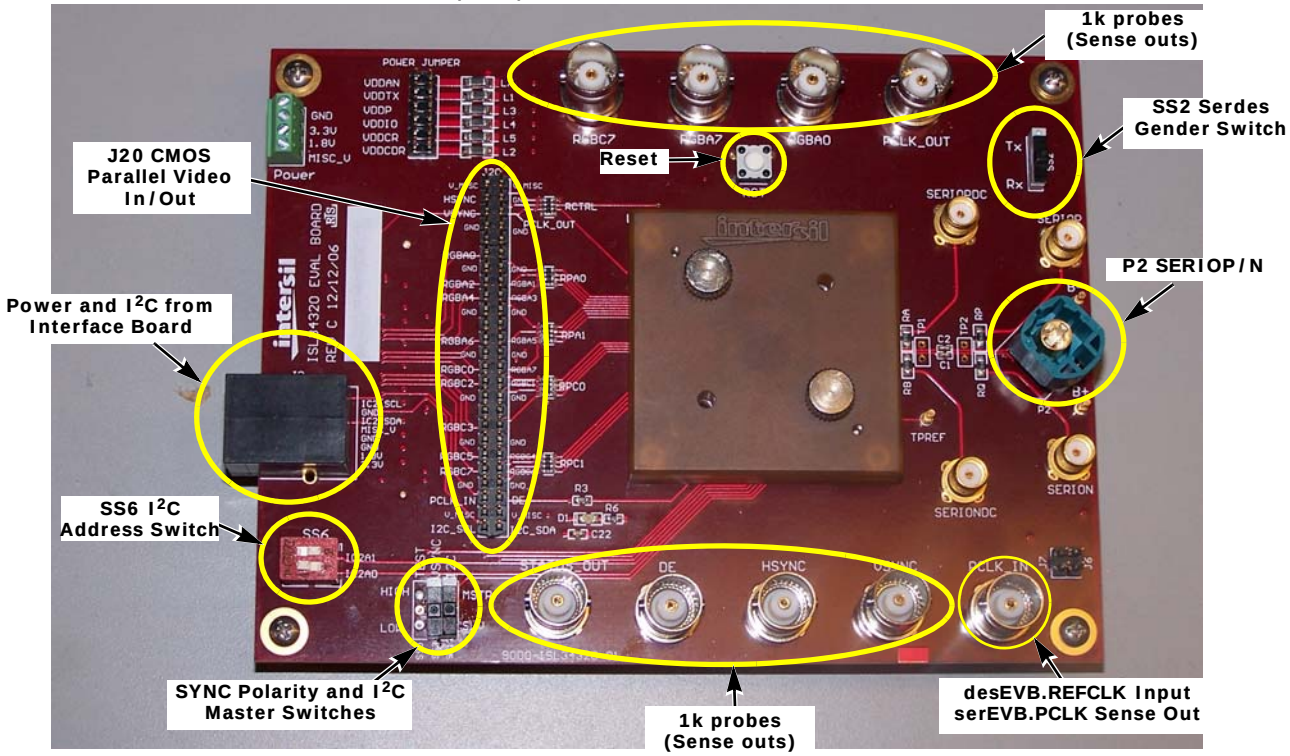


FIGURE 2. EVALUATION BOARD

1.3.1 Serdes Gender Selection

The gender of the serdes is set by the SS2 switch (as shown in Table 2) and come preset from the factory. Although the serdes and EVBs are interchangeable for video serialization and deserialization functions, there are two differences to keep in mind:

Rosenberger connector polarity. Due to the design of the Rosenberger HSD cable, signals fed in pins 1 and 3 come out at pins 2 and 4. To accommodate this, one of the evaluation boards has P2 rotated 90°. By convention, this is the deserializer EVB.

PCLK_IN BNC on the desEVB is an *input* to hook up an external function generator to supply the REFCLK to the deserializer. For the serEVB, this BNC is a sense output to monitor incoming ser.PCLK.

TABLE 2. SS2 SETTINGS

Ss2 Setting	Serdes Function	Evaluation Board Name
TX	video serializer	serEVB
RX	video deserializer	desEVB

1.3.2 Powering EVB

The EVB provides as direct access as possible to all the pins. As such, there are no power protection devices.

Misapplied power (reverse, overvoltage) can severely damage the serdes.

The EVB may be powered in any **one** of the following manners:

1. J2, the “Ethernet” connector. This is the default method using the Interface Board provided.
2. Green POWER terminal block.
3. J1, the 100 pin stacking connector.

TABLE 3. EVB POWER NODES

Power Node	Silkscreen Labels	Function
VDD1V8	1.8V	Serdes supply
VDD3V3	3.3V	Serdes supply
V_MISC	MISC_V	J20 (usually to power LCD panel), STATUS LED, crystal oscillator

The VDD1V8 and VDD3V3 are further split into individual domains for each of the supply pins on the serdes. The 6x2 header labeled “POWER JUMPER” provides a convenient place to monitor the voltages. The current of each supply pin can be individually measured by cutting the shorting traces on the back of the board opposite this jumper.

1.3.3 BNC Sense Outputs (Built-in 1k Probes)

Critical signals are “probed” by 950Ω resistors and brought to BNC and SMA connectors. When connected to a scope set to 50Ω inputs, these form a “built-in 1k probe” that allows the viewing of these signals with high fidelity -- as if one were probing right at the pins of the device. The built-in probes side-step the hassle of clip-type probes with ground clips. Furthermore, all of the built-in probes are matched to maintain their timing relationships relative to each other.

When using a scope of the proper bandwidth (generally >1GHz), rise times and signal integrity of the probed signal are not degraded. Lower frequency scopes may be used for debugging when only functionality matters and signal integrity is of secondary concern.

The built-in 1k probes form a resistor divider with the 50Ω input of the scope and attenuate the signal by a factor of 20. Therefore, a convenient setting is at 100mV/div, which translates to 2V/div.

1.3.4 J20 50 Pin Header For External Hookup

J20 is the 50 pin header that provides access to all of the pins on the serdes, except for SERIOP/N. Uses include:

- Connecting external RGB generator or LCD
- Hooking a scope probe tip
- Connecting to logic analyzer

1.3.5 J1 100 Pin Header For External Hookup

J1 is a stacking board-to-board connector providing same connectivity as J20. The mating connector is AMP 5-179031-4.

1.3.6 DesEVB.PCLK_IN BNC

The PCLK_IN BNC is not terminated for compatibility reasons and thus looks like a high-impedance input with direct connection to des.PCLK_IN. Lab function generators generally have 50Ω source impedance and assume a 50Ω load. Therefore, when driving a high impedance, the actual voltages will be double the instrument setting. ***3V setting = 6V actual***!

To avoid accidentally overvoltaging the serdes.PCLK_IN, use an inline BNC terminator or solder on a 50Ω resistor at RCIT location.

If a 50Ω resistor is soldered at RCIT, just be aware of this load when driving from J20 or J1. Most CMOS drivers cannot drive such a low load.

1.3.7 SerEVB.PCLK_IN BNC

This is a 1k sense output. To change it to an input, replace RCI1 with a 0Ω jumper. Same cautions in driving DesEVB.PCLK_IN apply.

1.3.8 Crystal

The 6 pin footprint Y1 can accommodate 5mmx7mm crystal oscillators of either 6 pin (Epson SG-9001CA series) or 4 pin (Abracon ASV series). Please consult the serdes technical brief for proper selection of the crystal oscillator. Specifically, the existence of spread spectrum switch on the evaluation board does not imply that the serdes will work with spread spectrum clocking.

The JP3 resistor jumper should be moved to complete the path between des.PCLK_IN and the crystal. From the factory, JP3 is connecting J20 and J1 to des.PCLK_IN.

1.4 Interface Board

The interface board shown in Figure 3 provides:

1. 3.3V and 1.8V power to evaluation boards from a single external 3.3V supply.
2. USB to I^2C bridge for PC.

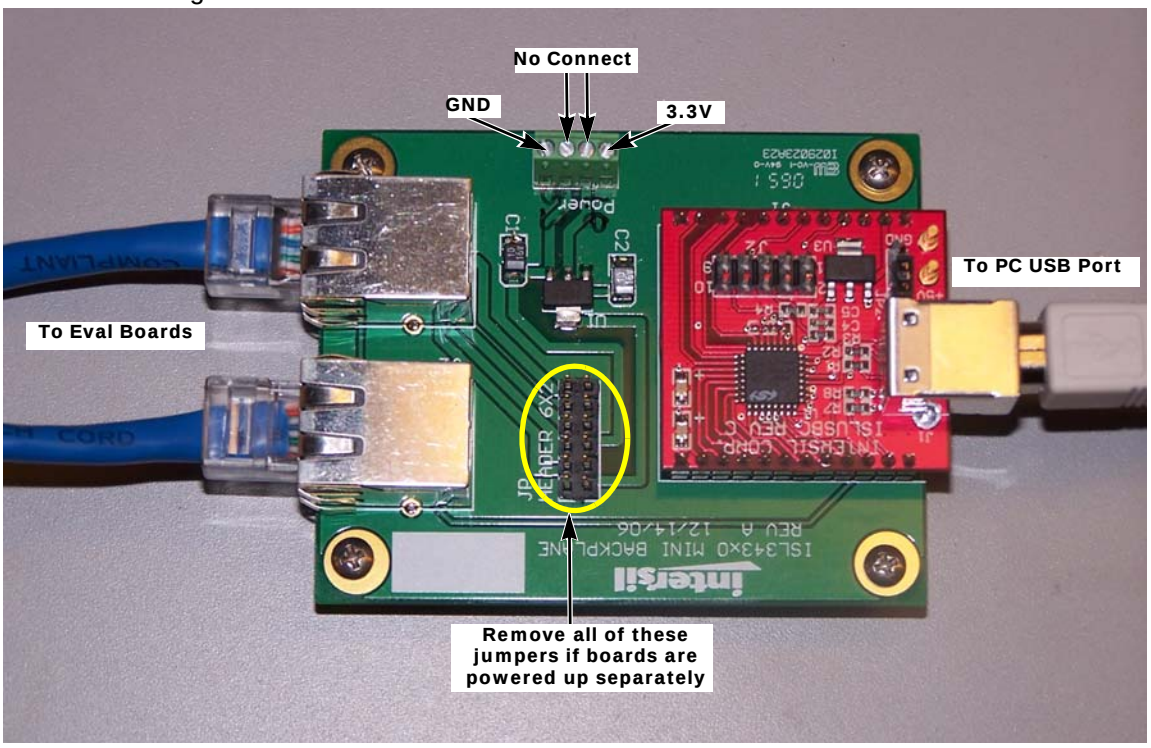


FIGURE 3. INTERFACE BOARD

Power and I^2C are distributed to the evaluation boards via the CAT5 cables, chosen for their wide availability (there are no high speed signals in these cables).

To power the evaluation boards from the interface board, all the jumpers in the 6x2 header must be installed. When powering the evaluation boards by other means, these jumpers **must be removed** to disconnect the power coming from the interface board if the interface board will still be used to provide connection to the PC.

2 Setup

2.1 Evaluation Board Setup

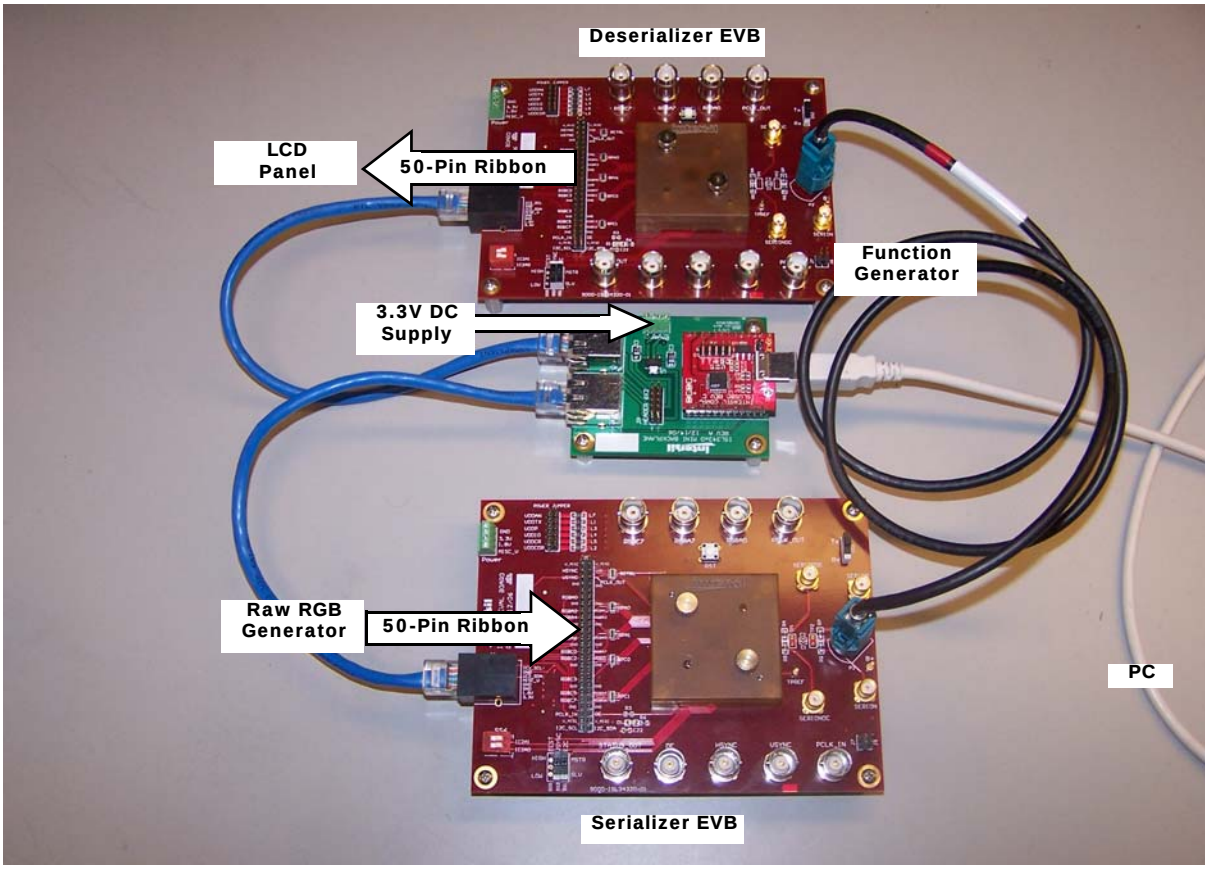


FIGURE 4. MAIN SETUP CONNECTIONS

- Raw RGB generator to serEVB.J20 through user's ribbon cable
- LCD panel or (other sink) to desEVB.J20 through user's ribbon cable
- 3.3V DC supply to Interface Board
- PC to Interface Board via USB cable
- SerEVB and desEVB to interface board via Ethernet cables
- SerEVB and devEVB via Rosenberger cable

It is almost redundant to mention that in this system, if any of the components are not working properly, or not connected, the result is "there is no image" or "I can't communicate via I^2C". The remaining subsections help the user ensure that each component is set up properly. Conversely, when things don't work, this section would be a good debug guide.

2.2 VSYNC/HSYNC Polarity Setup

For the serializer to transport video properly, it must know the polarity of the VSYNC and HSYNC signals supplied by the RGB driver. Symptoms of improper polarity setting can range from no transport to partial transport (missing colors).

Check and adjust VSYNC and HSYNC polarity on serEVB as follows:

1. Connect external RGB driver to J20.
2. Connect scope to HSYNC and VSYNC BNCs.
3. SS4 and SS3 switches should be set in HIGH position for the active low polarities seen in Figure 5:

FIGURE 5. ACTIVE LOW POLARITY EXAMPLE

4. SS4 and SS3 switches should be set in LO position for the active high polarities seen in Figure 6.

FIGURE 6. ACTIVE HIGH POLARITY EXAMPLE

On the desEVB, SS4 and SS3 control the deserializer's VSYNC and HSYNC output polarities.

2.3 PCLK Polarity Setup

A grainy or intermittent image is usually due to improper PCLK polarity. The serEVB.PCLK_IN and des.PCLK_OUT BNCs provide a convenient way to see the PCLK edge accurately in relation to the RGB, VSYNC, HSYNC, DE signals. The serdes can adjust PCLK active edge only via I^2C register setting.

2.4 I^2C Local Access

To set registers locally via I^2C, the following must be in place:

- des.PCLK_IN (REF_CLK) must be supplied to the desEVB via BNC, J20, or J1
- ser.PCLK_IN must be supplied to serEVB via J20 or J1 (not BNC)
- SS1 must be set to SLV position.
- Set I^2C address of serEVB to 0x60 (all SS6 dip switches set to 0)
- Set I^2C address of desEVB to 0x62 (SS6 dip switch IC2A0 = 1 all others set to 0)

2.5 GUI Installation

The GUI allows setting and viewing the serdes I2C registers from the PC. To install:

1. Unzip Intersil_I2C_Comm_Installer_V310_The_password_is_c.zip
2. Run file Intersil_I2C_Comm_Installer_V310.exe
3. Move file Intersil_I2C_Comm_V311.exe to the installation directory and create a shortcut.

3 Quickstart

Assuming a raw RGB source is hooked up to J20, this section provides a sample start-up procedure.

TABLE 5. SCOPE SETUP FOR BOARD DEBUG

Channel	Signal	Connection type
Ch1	ser.PCLK_IN	BNC
Ch2	ser.DE	BNC
Ch3	ser.VSYNC	BNC
Ch4	des.VSYNC	BNC

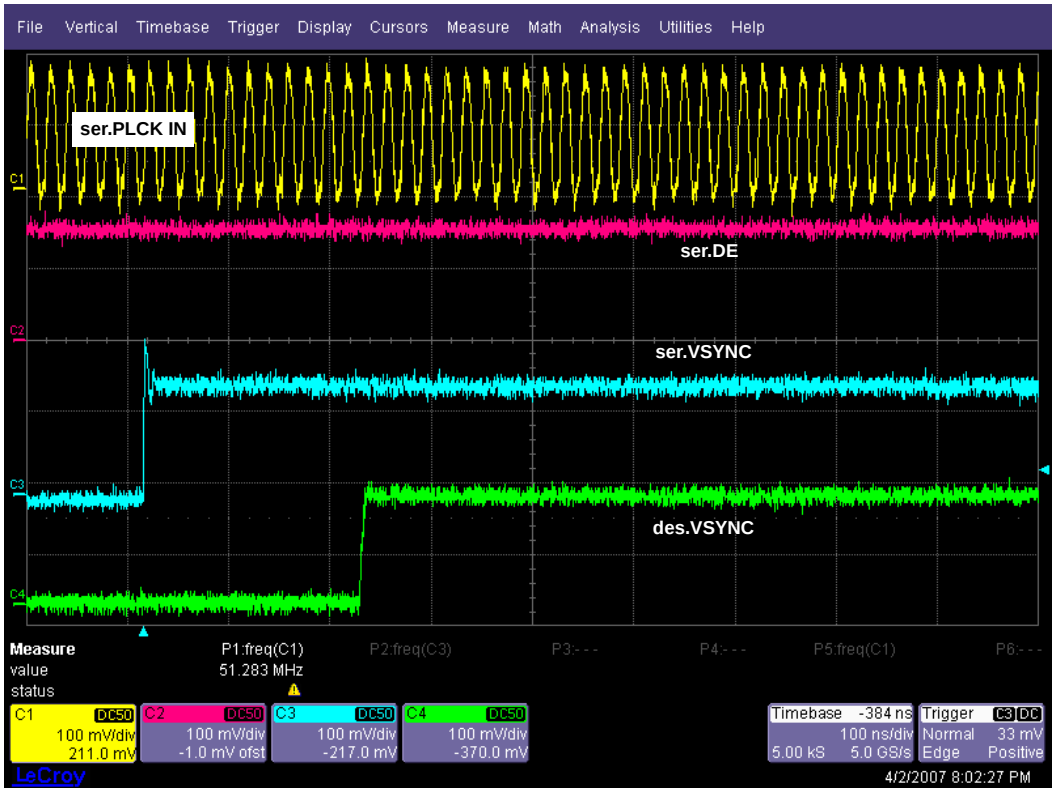


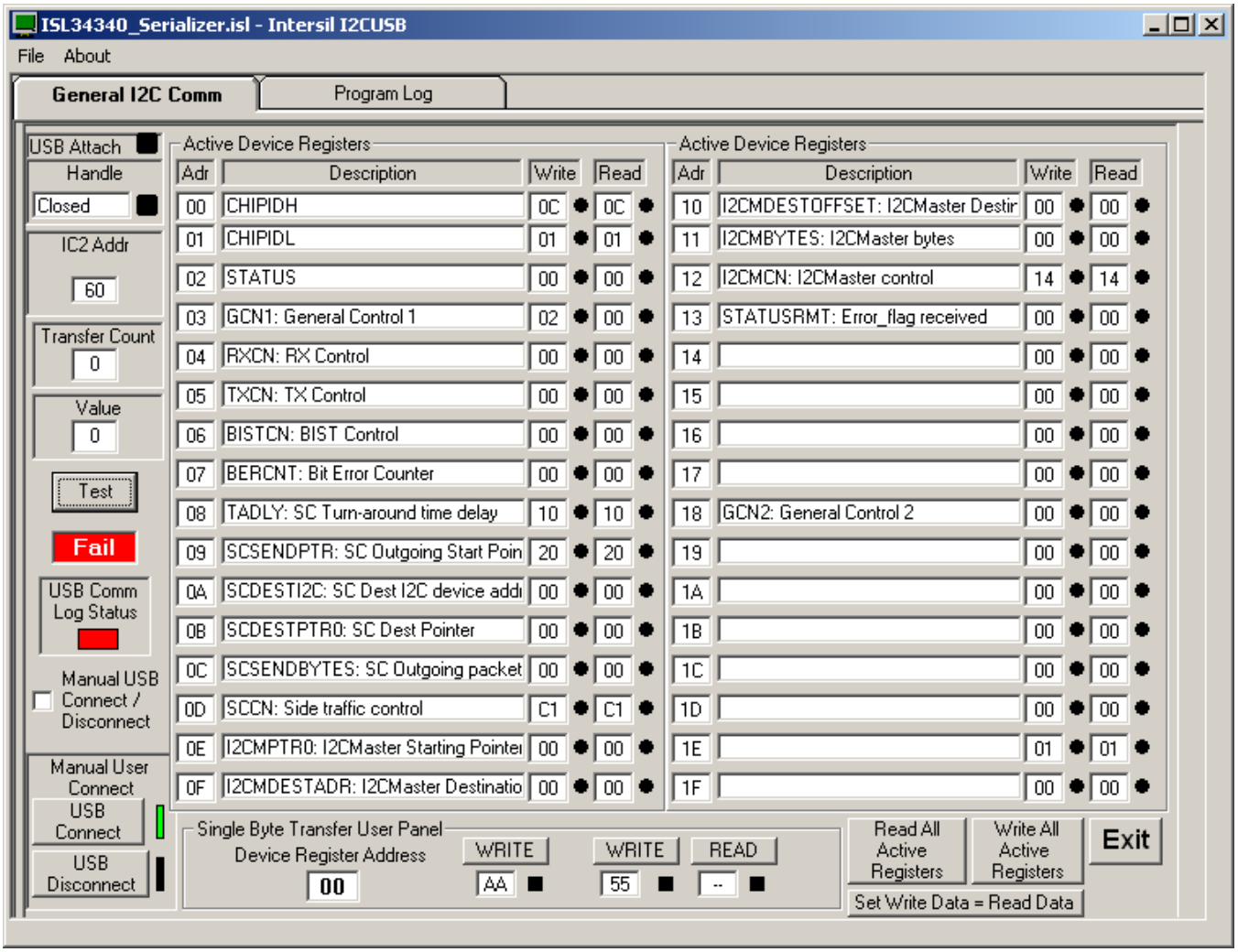
FIGURE 7. SCREEN SHOT OF WORKING SETUP

1. Scope settings
   - •All channels 100mV/div, DC 50Ω coupling
   - •Time base 100ns/div
   - •Trigger on rising edge of Ch3 (ser.VSYNC)
   - •Measure Ch1 frequency (ser.PCLK_IN)
2. External function generator to provide REFCLK
   - •Connect to des.PCLK-IN through BNC cable.
   - •Set function generator to the measured frequency from scope Ch1 (ser.PCLK_in).
   - •Set amplitude to 1.0V (refer to section 1.3.6 for caution)
   - •Enable function generator output.
   - •Press RESET button on des.EVB

4 GUI Usage

Open two instances of the GUI so that one controls the serializer and another the deserializer. The two GUIs will communicate through the same Interface Board. Register file definitions set the “personality” of the generic GUI.

- Open the GUI “Intersil_I2C_Comm_V311.exe”
- Load ISL34340_Serializer.isl (File->Open->Comm Register Definitions)



- Make sure I^2C Addr matches the value of the serEVB
- Click on TEST button and make sure the box below it turns green. You must click on the TEST button if the I^2C Addr is changed.
- Open a second GUI “Intersil_I2C_Comm_V311.exe”
- Load a register map definition ISL34340_Deserializer.isl